

PTO/SB/08A

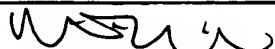
INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

Sheet 1 of 1

Application Number.: Unassigned 10/777,262  
 Filing Date: Herewith 2/12/4  
 First Named Inventor: Craig M. Darsow  
 Art Unit: Unassigned 2825  
 Examiner Name: Unassigned GARGOWSKI  
 Attorney Docket Number.: ROC920030333US1

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and or country where published.	T <sup>2</sup>
WP		Patent Application entitled "Apparatus and Method for Performing Static Timing Analysis of an Integrated Circuit Design Using Dummy Edge Modeling," Craig M. Darsow et al., filed February 12, 2004.	

Examiner Signature		Date Considered	3/1/6
--------------------	---	-----------------	-------

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through  
 citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional).

<sup>2</sup> Applicant is to place a check mark here if English language translation is attached.